REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 5-9 and 12-22 are all the claims presently pending in the application. Claims 5-7, 12-15, 18 and 21-22 have been amended to more particularly define the invention. Claims 1-4 and 10-11 have been canceled.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 6 and 13 stand rejected upon informalities (e.g., 35 U.S.C. § 112, first paragraph). Claims 5, 8, 12, 15, 18 and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Seo, et al. (U.S. Patent No. 5,981,324). Claims 6-7, 9, 13-14, 16-17, 19 and 21-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Seo, et al.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined by claim 5 is directed to a method of manufacturing a DRAM-incorporated semiconductor device in which a DRAM section and a logic section are formed on a semiconductor substrate that is isolated into elements. The method includes forming a metal film including one of cobalt and nickel directly on surfaces of highly doped source-drain regions and gate regions in the DRAM section and the logic section, and heat treating the device to react the metal film with the surfaces to concurrently form a metal silicide layer in each of the DRAM section and the logic section.

In conventional methods, if a high-concentration impurity layer is formed in source/drain (S/D) regions of DRAM cell section and a titanium silicide layer is formed thereon, crystalline defects occur in the high-concentration source/drain regions and these defects can increase junction leakage current. Therefore, the titanium silicide layer is formed on the lightly doped S/D regions in the DRAM cell section to reduce the crystalline defects.

The claimed invention, on the other hand, forms a metal film including one of cobalt

and nickel directly on surfaces of highly doped source-drain regions and gate regions in the DRAM section and the logic section. Unlike titanium silicide, when cobalt or nickel silicide is used, crystal defects do not generate in the S/D regions of DRAM cell section.

II. THE 35 USC §112, FIRST PARAGRAPH REJECTION

Claims 3 and 6 stand rejected under 35 U.S.C. §112, first paragraph. Applicant notes, however, that the claims have been amended to address the Examiner's concerns. Specifically, these claims have been amended to recite "*wherein said heat treating comprises: heating said device at 500-600 ℃; removing unreacted metal film with a mixed solution of sulfuric acid and hydrogen peroxide; and heating said device at 800 ℃*". Thus, these claims clearly include "removing unreacted metal film" as part of the "heat treating" as described in the specification (Application at page 11, lines 1-2).

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE SEO REFERENCE

The Examiner alleges that Seo teaches the claimed invention of claims 5, 8, 12, 15, 18 and 20, and makes obvious the invention of claims 6, 7, 9, 13, 14, 16, 17, 19, 21 and 22. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Seo.

Seo discloses a method of forming integrated circuits having memory cell arrays and peripheral circuits. The method includes forming a first well region of first conductivity type in a memory cell portion and a second well region of first conductivity type in a peripheral circuit portion extending adjacent the memory cell portion. First and second insulated gate electrodes are then formed on the first and second well regions, respectively, using conventional techniques. First dopants of second conductivity type are then implanted at a first dose level into the first and second well regions, using the first and second insulated gate electrodes as an implant mask. These dopants are then diffused to form lightly doped source and drain regions adjacent the first and second insulated agate electrodes. Second dopants of second conductivity type are then selectively implanted at a second dose level, greater than the first dose level, into the second well region using self-alignment techniques. However,

these dopants are preferably not implanted into the first well region. The second dopants are then diffused into the second source/drain regions (Seo at Abstract).

However, contrary to the Examiner's allegations, Seo does not teach or suggest "*forming a metal film comprising one of cobalt and nickel directly on surfaces of highly doped source-drain regions and gate regions in said DRAM section and said logic section*", as recited, for example, in claims 5, 12 and 15.

As noted above, unlike conventional methods which form a titanium silicide layer on the lightly doped S/D regions in the DRAM cell section to reduce the crystalline defects, the claimed invention, on the other hand, forms a metal film including one of cobalt and nickel directly on surfaces of highly doped source-drain regions and gate regions in the DRAM section and the logic section (Application at page 10, line 15-page 11, line 8). Unlike titanium silicide, when cobalt or nickel silicide is used, crystal defects do not generate in the S/D regions of DRAM cell section (Application at page 12, line 18-page 13, line 14).

In particular, the claimed method may form the metal film directly on the surface of highly-doped source-drain regions and gate regions, and react the metal film with surface to form a metal silicide (Application at Figure 6; page 10, lines 15-21). The source-drain regions may, therefore, be formed with a high dopant concentration, and a leakage current may be substantially eliminated (Application at page 12, line 18-page 13, line 14).

Specifically, it is explained that "[w]hat distinguishes the present invention from the conventional techniques the most is the fact that, even in the memory cell region of the DRAM section, there are formed the S/D regions with a high dopant concentration defined as n^+. **When silicide is formed on the S/D regions with such a high dopant concentration, good ohmic contacts can be formed.** Further, because the junction becomes deeper, the junction leakage current is hardly generated even if silicide is formed over all the surfaces of the S/D regions. In contrast with this, **when silicide is formed on conventional low dopant-concentration regions (n^-), Schottkey contacts are formed therebetween,** which is not adequate for the purpose of achieving lower resistance (Application at page 12, line 18-page 13, line 6) (Emphasis added).

Clearly, these features are not taught or suggested by Seo. Indeed, with the conventional technology of the Seo reference, if a high-concentration impurity layer is formed in source/drain (S/D) regions of DRAM cell section and a titanium silicide layer is formed

thereon, crystalline defects occur in the high-concentration source/drain regions and these defects can increase junction leakage current. Thus, Seo forms a titanium silicide layer on the lightly doped S/D regions in the DRAM cell section to reduce the crystalline defects.

The present invention, on the other hand, uses cobalt or nickel silicide (and not titanium silicide) on the highly-doped S/D regions of the DRAM cell section. Therefore, crystal defects are not generated in the S/D regions of the DRAM cell section in the present invention.

It is thought that this may be based (at least in part) on the difference between reaction temperatures at the time of silicidation reaction and the difference of structures of formed crystals. That is, the reactivity of titanium with silicon greatly differs from the reactivity of cobalt or nickel with silicon. According to the higher reactivity, cobalt is converted to CoSi at 500-600°C and after removing an unreacted metal film in this stage, CoSi is further reacted with silicon to produce $CoSi_2$ by heating again (about 800°C). On the other hand, in the case of titanium, high reaction temperature (650°C or more) is needed because of lower reactivity with silicon.

Moreover, since a lattice constant of a cobalt silicide crystal is similar to that of a silicon single crystal of a substrate, the cobalt silicide crystals are grown similar to epitaxial growth. In contrast, since a lattice constant of a titanium silicde crystal differs greatly from that of a silicon single crystal, there is a problem that a crystalline boundary is formed. Further, since the high temperature is still required in the case of titanium, the crystal grain size also becomes large, especially, with a rule of 0.2 micrometers or less of these days, there is also a problem that a stable film cannot be formed.

Nickel has very similar properties to those of cobalt because nickel and cobalt are classified into the eighth group in the Periodic Table. On the other hand, titanium is classified into the fourth group in the Periodic Table and greatly differs in properties from cobalt.

In order to prove the above fact, the present inventor formed a titanium silicide, cobalt silicide, and nickel silicide in DRAM cell section manufactured with a rule of 0.18 micrometer, respectively, and examined the voltage dependability of leakage current in N^+ diffusion layer. The results are illustrated in the graph in the Exhibit 1 which is attached hereto and incorporated by reference herein.

In the graph of Exhibit 1, leakage current [A/μm²] is shown in an ordinate axis, and opposite direction bias (voltage at the side which measures leakage current) is shown in the horizontal axis. As illustrated in the graph, in the case of titanium silicide, leakage current increases on low voltage as compared with cobalt silicide and nickel silicide. In addition, although two curves are shown for titanium silicide, since it varied greatly when carried out twice, in order that this might look at reproducibility, it is shown that a reproducible film was not obtained. In the cases of cobalt silicide and nickel silicide, film formation was reproducibly carried out, and one graph curve being expressed, respectively.

In an actual device, leakage current at low voltage (about 2-3V) is a bad influence on the device. Therefore, if leakage current at low voltage increases, hold characteristics (i.e., refresh characteristics indicated in this reference) of the DRAM decreases.

At the time of filing the Seo reference, titanium silicide was mainly used in the industry as a silicide. Further, although it was known that cobalt and nickel could also be formed into silicide, the difference between cobalt or nickel silicide, and titanium silicide was not considered. Therefore, even if the silicide could be formed on highly doped S/D regions in DRAM cell section, leakage current was considerably high. As described in the present specification, conventionally it was common sense that S/D regions in a DRAM section must be made of low concentration for inhibition of a short channel effect and relaxation of drain electric field. Although there are some proposals which form a silicide on lightly doped S/D regions similar to the Seo reference, a Schottky junction would be formed by having formed silicide on S/D regions with a shallow junction. As a result, good ohmic contact was not obtained.

Thus, against the teaching of conventional technologies, the inventors found that when a specific silicide (e.g., cobalt or nickel silicide) is formed, a phenomenon that leakage current increases is suppressed even if the silicide is formed on highly doped S/D regions. According to this foundation, high-speed operation is attained by good ohmic contact being realizable as compared with the reference.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Seo. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 5-9 and 12-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 11/20/03

Phillip E. Miller, Esq.
Registration No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Douglas Owens, Group Art Unit # 2811 at fax number (703) 872-9319 this 20th day of November, 2003.

Phillip E. Miller
Reg. No. 46,060

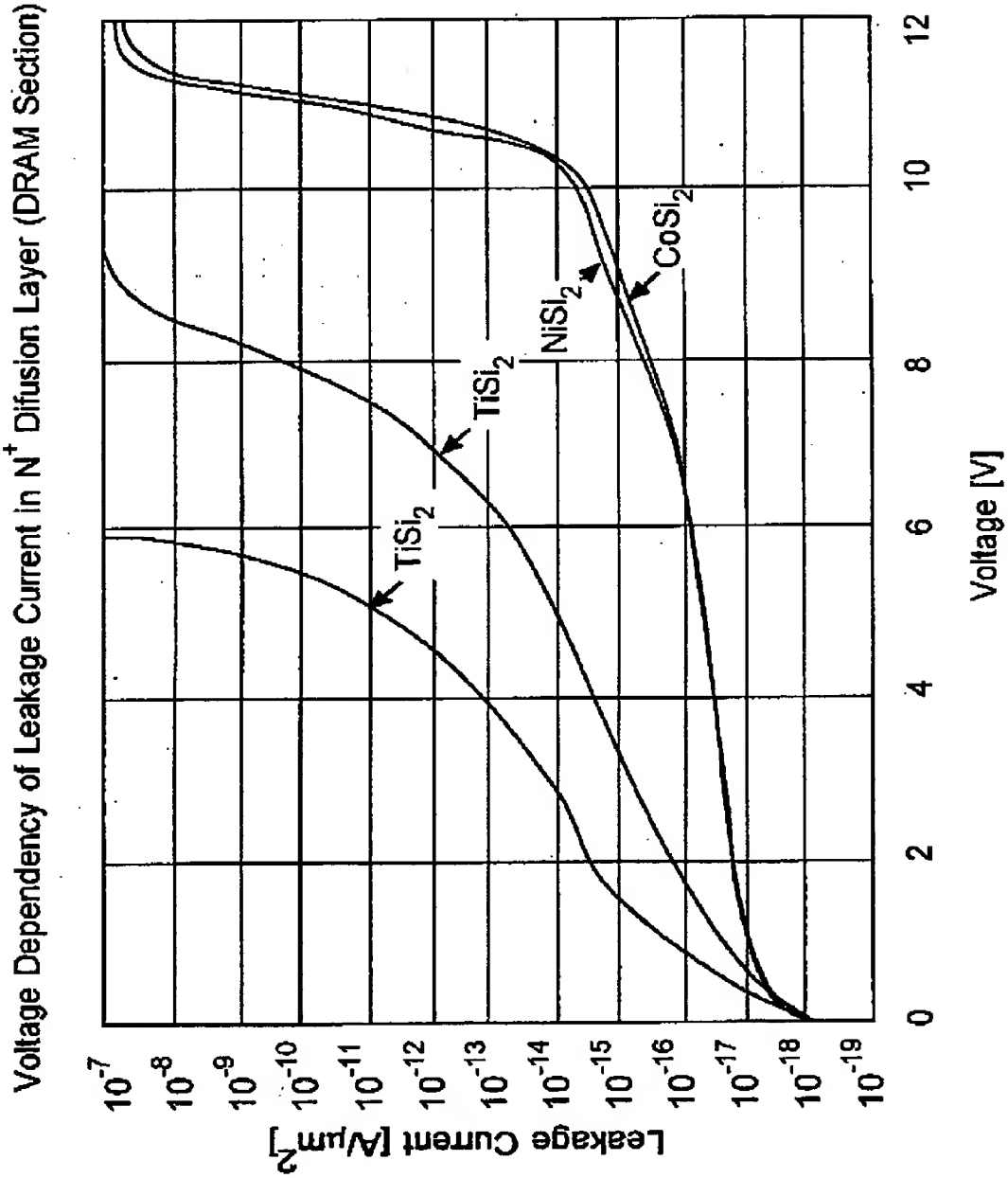
Voltage Dependency of Leakage Current in N+ Difusion Layer (DRAM Section)
Leakage Current [A/μm2]
10-7
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
10-16
10-17
10-18
10-19
0
2
4
6
8
10
12
Voltage [V]
TiSi2
TiSi2
NiSi2
CoSi2

Exhibit 1